Amendments to the claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of claims:

Claim 1 (currently amended): A semiconductor package with a heat sink, comprising:

a substrate having a top surface and an opposite bottom surface;

at least one chip disposed on the top surface of the substrate and electrically connected to the substrate via a plurality of conductive elements;

a heat sink mounted on the top surface of the substrate and connected to the chip, wherein the heat sink has a top surface and an opposite bottom surface and comprises a flat portion attached to the chip, a support portion extending from an edge of the flat portion to the substrate, and a bonding portion extending laterally from an end~~, extending to the substrate,~~ of the support portion and connected to the substrate, allowing the flat portion to be supported and elevated above the chip by the support portion, and allowing the bonding portion to be attached to the top surface of the substrate, with at least one slot formed through at least one corner of the bonding portion to expose the top surface of the substrate, the slot comprising a through hole penetrating the top and bottom surfaces of the bonding portion of the heat sink;

an adhesive material applied between the bonding portion of the heat sink and the top surface of the substrate and filled in the slot through the corner of the bonding portion with an overflow of the adhesive material out of the slot, so as to attach the heat sink to the substrate by means of the adhesive material; and

a plurality of solder balls mounted on the bottom surface of the substrate.

Claim 2 (original): The semiconductor package of claim 1, wherein the adhesive material is an adhesive.

Claim 3 (original): The semiconductor package of claim 1, wherein the adhesive material is solder.

Claim 4 (original): The semiconductor package of claim 1, wherein the substrate is made of a material selected from the group consisting of epoxy resin, polyimide, BT (bismaleimide triazine) resin, and FR4 resin.

Claim 5 (original): The semiconductor package of claim 1, wherein the chip has an active surface and an opposite non-active surface, allowing the plurality of conductive elements to be bonded to the active surface of the chip and the top surface of the substrate to electrically connect the chip to the substrate.

Claim 6 (original): The semiconductor package of claim 5, wherein the conductive elements are solder bumps.

Claim 7 (original): The semiconductor package of claim 6, wherein an insulating material is applied between the chip and the substrate to fill up gaps between the adjacent solder bumps.

Claim 8 (original): The semiconductor package of claim 1, wherein the heat sink is made by stamping a thermally conductive material.

Claim 9 (original): The semiconductor package of claim 1, wherein the flat portion of the heat sink is attached to the chip via an adhesive.

Claim 10 (original): The semiconductor package of claim 9, wherein the adhesive is a thermally conductive adhesive.

Claim 11 (original): The semiconductor package of claim 1, wherein the adhesive material filled in the slot is shaped as a rivet to provide an anchoring effect.

Claim 12 (original): The semiconductor package of claim 1, wherein the slot is of a I-shape in a horizontal sectional view thereof.

Claim 13 (original): The semiconductor package of claim 1, wherein the slot is of a triangular shape in a horizontal sectional view thereof.

Claim 14 (original): The semiconductor package of claim 1, wherein the slot is of a cross shape in a horizontal sectional view thereof.

Claim 15 (original): The semiconductor package of claim 1, wherein the slot is of a hemispherical shape in a horizontal sectional view thereof.

Claim 16 (original): The semiconductor package of claim 1, wherein the slot is of a T-shape in a horizontal sectional view thereof.

Claim 17 (original): The semiconductor package of claim 1, wherein the slot has a taper structure.

Claim 18 (original): The semiconductor package of claim 1, wherein an inner wall of the slot is bent to form a stepped structure.